Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 90413

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2022.

Fourth/Fifth/Seventh Semester

Computer Science and Engineering

CS 8491 — COMPUTER ARCHITECTURE

(Common to Computer and Communication Engineering/Electrical and Electronics Engineering/Robotics and Automation/Information Technology)

(Regulations 2017)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. State Amdahl's law.

2. Assume that for a given program 70% of the executed instructions are arithmetic, 10% are load/store, and 20% are branch. Given this instruction mix and the assumption that an arithmetic instruction requires 2 cycles, a load/store instruction takes 6 cycles, and a branch instruction takes 3 cycles, find the average CPI.

3. Discuss carry save adder with suitable example.

4. What is subword parallelism?

5. What are the disadvantages of the single cycle implementation of MIPS instruction unit?

6. Distinguish between a true data dependence and name dependence with suitable example.

7. What is coarse grained parallelism?

8. Define GPU. How does it vary from CPUs.

9. What is the role of write buffer in write through cache?

10. Write about interface circuits.

PART B — (5 × 13 = 65 marks)

11. (a) (i) Assume that a program runs in 100 seconds on a machine, with multiply operations responsible for 80 seconds. How much do I have to improve the speed of multiplication if I want my program to run 2 times faster? (5)

(ii) Write the MIPS assembly language to compute the sum of odd numbers up to the largest odd number smaller than or equal to n, e.g. 1 + 3 + 5 + ... +n (Or n – 1 if n is even). Assume Register 4 contains n, a positive integer. Put the output in Register 2. (8)

Or

(b) (i) Discuss the operations performed by the following instructions and discuss the addressing modes used (3)

```
add $t0, $s6, $s4
addi $t1, $s4, 10
sw $t1, 0($t0)
```

(ii) Discuss the format and addressing modes used in MIPS branching instruction with suitable example. (10)

12. (a) Explain the division algorithm in detail with diagram and examples. (13)

Or

(b) Explain floating point addition with a neat diagram of ALU unit. (13)

13. (a) (i) What is pipelining? Discuss about pipelined data path control. (8)

(ii) Discuss the MIPS implementation of the data path control for the instruction SW R1, 1000(R2), with neat diagram, Clearly indicate the flow of data. (5)

Or

(b) (i) How does MIPS handle exceptions? (5)

(ii) What is meant by dynamic branch prediction? Discuss the different branch prediction schemes with suitable example. (8)

14. (a) Explain the four different approaches to multithreading with necessary diagrams. (13)

Or

(b) (i) What are the challenges in parallel processing? (8)

(ii) Classify shared memory multiprocessor based on the memory access latency. (5)

15. (a) (i) What is TLB? Discuss its usage. (5)

(ii) Discuss the concept of paging and how a paged memory management system is implemented. (8)

Or

(b) Explain DMA controller with block diagram. What are the advantages of a DMA transfer compared to interrupt driven transfer? (13)

PART C — (1 × 15 = 15 marks)

16. (a) Consider the following loop : (15)

```
loop : lw r1, 0(r1)
       and r1, r1, r2
       lw r1, 0(r1)
       lw r1, 0(r1)
       beq r1, r0, loop
```

Assume that perfect branch prediction is used and no stalls due to control hazards, that there are no delay slots, and that the pipeline has full forwarding support. Also assume that many iterations of this loop are executed before the loop exits.

Show a pipeline execution diagram for the third iteration of this loop, from the cycle in which we fetch the first instruction of that iteration up to (but not including) the cycle in which we can fetch the first instruction of the next iteration. Show all instructions that are in the pipeline during these cycles.

Or

(b) (i) Define cache memory. Explain the various mapping techniques associated with cache memories. (10)

(ii) A block-set associative cache memory consists of 128 blocks divided into four block sets. The main memory consists of 16,384 blocks and each block contains 256 eight bit words.

How many bits are required for addressing the main memory?

How many bits are needed to represent the TAG, SET and WORD fields? (5)